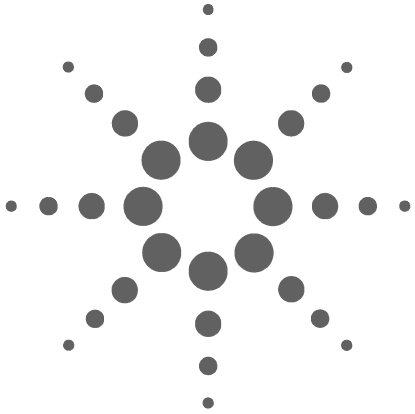

Agilent TS-5400 Functional Test System Series IIB

Agilent E6174A 32-Channel Event Detector User's Manual

Manual Part Number E6174-90021

Agilent Technologies

Notices

Documentation History

All Editions and Updates of this manual and their creation date are listed below. The first Edition of the manual is Edition 1. The Edition number increments by 1 whenever the manual is revised. Updates, which are issued between Editions, contain replacement pages to correct or add additional information to the current Edition of the manual. Whenever a new Edition is created, it will contain all of the Update information for the previous Edition. Each new Edition or Update also includes a revised copy of this documentation history page.

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Safety Notices

Caution

A **Caution** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **Caution** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Safety Summary

The following general safety precautions must be observed during all phases of operation of this system. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the system. Agilent Technologies, Inc. assumes no liability for the customer's failure to comply with these requirements.

General

This product is provided with a protective earth terminal. The protective features of this product may be impaired if it is used in a manner not specified in the operation instructions.

WARNING: DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or flames.

If the equipment in this system is used in a manner not specified by Agilent Technologies, the protection provided by the equipment may be impaired.

Cleaning Instructions

Clean the system cabinet using a soft cloth dampened in water.

WARNING: DO NOT REMOVE ANY SYSTEM COVER

Operating personnel must not remove system covers. Component replacement and internal adjustments must be made only by qualified service personnel. Equipment that appears damaged or defective should be made inoperative and secured against unintended operation until they can be repaired by qualified service personnel.

Environmental Conditions

Unless otherwise noted in the specifications, this system is intended for indoor use in an installation category II, pollution degree 2 environment. It is designed to operate at a maximum relative humidity of 80% and at altitudes of up to 2000 meters. Refer to the specifications tables for the ac mains voltage requirements and ambient operating temperature range.

Before applying power

Verify that all safety precautions are taken. Note the external markings described in “Safety Symbols and Regulatory Markings” on page 4.

Ground the System

To minimize shock hazard, the system chassis must have a hard-wired connection to an electrical protective earth ground. The system must also be connected to the ac power mains through a power cable that includes a protective earth conductor. The power cable ground wire must be connected to an electrical ground (safety ground) at the power outlet. Any interruption of the protective grounding will cause a potential shock hazard that could result in personal injury.

Fuses

Use only fuses with the required rated current, voltage, and specified type (normal blow, time delay). Do not use repaired fuses or short-circuited fuse holders. To do so could cause a shock or fire hazard.

Operator Safety Information

MODULE CONNECTORS AND TEST SIGNAL CABLES CONNECTED TO THEM CANNOT BE OPERATOR ACCESSIBLE: Cables and connectors are considered inaccessible if a tool (e.g., screwdriver, wrench, socket, etc.) or a key (equipment in a locked cabinet) is required to gain access to them. Additionally, the operator cannot have access to a conductive surface connected to any cable conductor (High, Low or Guard).

ASSURE THE EQUIPMENT UNDER TEST HAS ADEQUATE INSULATION BETWEEN THE CABLE CONNECTIONS AND ANY OPERATOR-ACCESSIBLE PARTS (DOORS, COVERS, PANELS, SHIELDS, CASES, CABINETS, ETC.): Verify there are multiple and sufficient protective means (rated for the voltages you are applying) to assure the operator will NOT come into contact with any energized conductor even if one of the protective means fails to work as intended. For example, the inner side of a case, cabinet, door, cover or panel can be covered with an insulating material as well as routing the test cables to the module's front panel connectors through non-conductive, flexible conduit such as that used in electrical power distribution.

Safety Symbols and Regulatory Markings

Symbols and markings on the system, in manuals and on instruments alert you to potential risks, provide information about conditions, and comply with international regulations. Table 1 defines the symbols and markings you may encounter.

Table 1 Safety Symbols and Markings

Safety symbols	
	Warning: risk of electric shock.
	Caution: refer to accompanying documents.
	Alternating current.
	Both direct and alternating current.
	Earth (ground) terminal
	Protective earth (ground) terminal
	Frame or chassis terminal
	Terminal is at earth potential. Used for measurement and control circuits designed to be operated with one terminal at earth potential.
	Switch setting indicator. O = Off, | = On.
	Standby (supply); units with this symbol are not completely disconnected from ac mains when this switch is off. To completely disconnect the unit from ac mains, either disconnect the power cord, or have a qualified electrician install an external switch.
Regulatory Markings	
	The CE mark is a registered trademark of the European Community.
	The CSA mark is a registered trademark of the Canadian Standards Association.
 N10149	The C-tick mark is a registered trademark of the Spectrum Management Agency of Australia. This signifies compliance with the Australian EMC Framework regulations under the terms of the Radio Communications Act of 1992.
ISM 1-A	This text indicates that the product is an Industrial Scientific and Medical Group 1 Class A product (CISPR 11, Clause 4).

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Click the link to **Test & Measurement**. Select your country from the drop-down menus. The Web page that appears next has contact information specific for your country.

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If you do not have access to the Internet, call one of the numbers in Table 2.

Table 2 Agilent Call Centers and Regional Headquarters

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Europe:	(41 22) 780 8111
Japan:	Measurement Assistance Center (81) 0426 56 7832
Latin America:	305 269 7548
Asia-Pacific:	(85 22) 599 7777

Declaration of Conformity

According to ISO/IEC Guide 22 and EN 45014

Manufacturer's Name: Agilent Technologies
Loveland Manufacturing Center

Manufacturer's Address: 815 14th Street S.W.
Loveland, Colorado 80537

Declares, that the product:

Product Name: Agilent Technologies E6174A Event Detector
Model Number: Agilent E6174A
Product Options: All

Conforms to the following Product Specifications:

Safety: IEC 61010-1 (1990)+A2:1995/EN61010-1:1993+A2:1995
CSA C22.2 #1010.1 (1992)
UL 3111

EMC: CISPR 11:1990/EN55011 1991: Group 1, Class A
EN50082-1:1992
IEC 61000-4-2:1995/: 4kV CD
IEC 61000-4-3:1995/: 3V/m
IEC 61000-4-4:1995/: 1 kV Power line

Supplementary Information: This product complies with the requirements of the Low Voltage Directive 73/23/EEC (inclusive 93/68/EEC). This product also wherewith complies with the protection requirements of: The EMC Directive 89/336/EEC and carries the "CE" marking accordingly. Attestation is provided according to article 10(2) of the Directive by a Technical Construction File.

Technical File Number: 95-0900-002-TCF Rev. C Dated: 28 June, 1999

A Technical Report/Certificate has been issued by the following appointed Competent Body, namely,
KEMA Registered Quality Nederland B.V.
Utrechtseweg 310, 6812 AR Arnhem
6800 ET Arnhem, The Netherlands
Certificate Number: 71301-KRQ/EMC 97-4165 **Dated:** February 18, 1997

June 28, 1999

For Compliance Information ONLY, contact:

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European Contact: Your local Agilent Technologies Sales and Service Office or Agilent Technologies GmbH, Department HQ-TRE, Standards Europe, Herrenberger Straße 130, D-71034 Böblingen (FAX: +49-7031-14-3143)

USA Contact: Product Regulations Manager, Agilent Technologies Company, P.O. Box 301, Mail Stop BU212, Loveland, CO 80537

Notes:

Contents

Chapter 1
Getting Started

Using This Chapter

This chapter describes the Agilent E6174A 32-Channel Event Detector (formerly the Agilent Z2902A) and contains the following sections:

Description

Implemented as a single C-sized VXIbus module, it is a simple, FIFO register-based event detector module designed to record relative event changes across 32 channels and time stamp those changes for later analysis. This card is designed to satisfy the need for a signal analyzer in typical functional test measurements in an automotive electronics manufacturing environment.

Key features of the module include:

- 32 input signal channels.
- Programmable threshold value with 8 bit resolution for 8 channels independently.
- Four decades internal clock selection from 10 Khz to maximum of 10 MHz.
- Memory depth of 1024 events capturing the state of each input channel.
- 24 bit time tag for each event.
- Built-in input hysteresis.
- External Trigger input.
- External Clock input Start/Stop internal trigger capability.

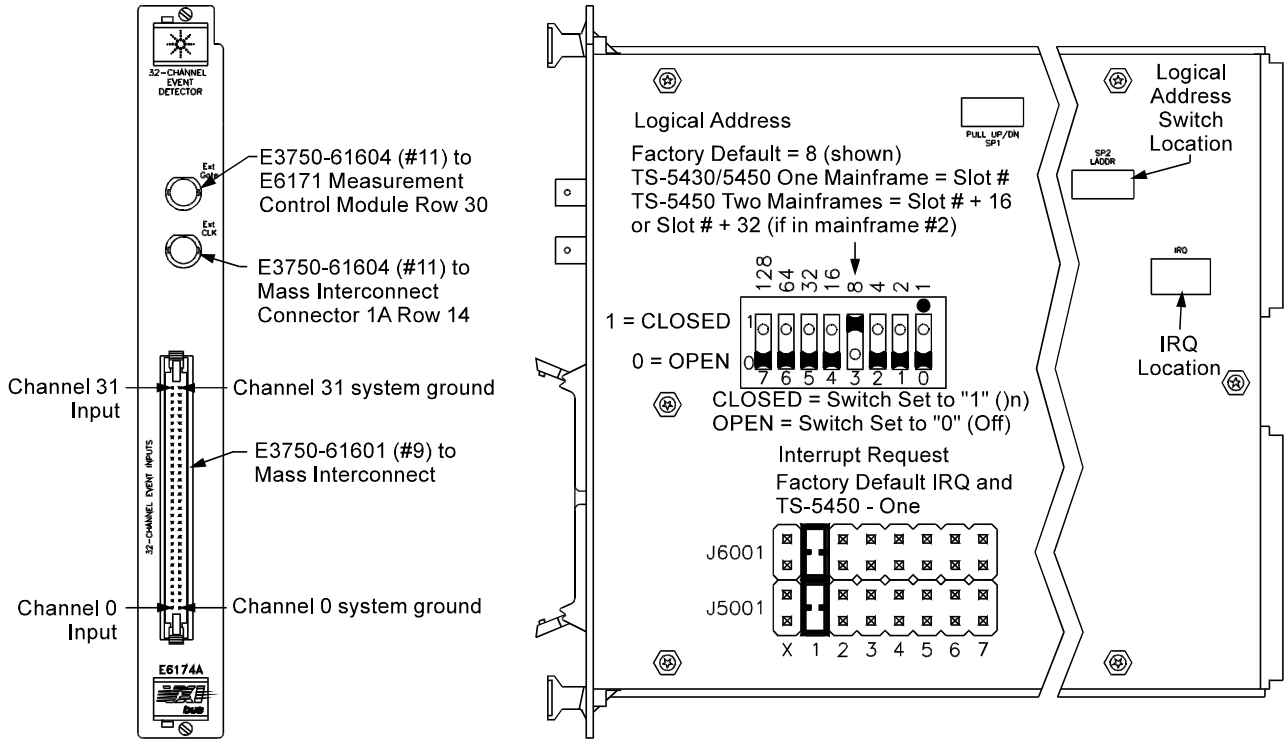

Figure 1-1. Agilent E6174A 32-Channel Event Detector

Note The Agilent E6174A Event Detector Module has:

Access ports on the side of the case for manually setting the IRQ and the Logical address (LADDR).

The indicated Pull Up/Down switch SP1 has been removed and replaced by 8 jumper wires. You can physically install Pull Up/Down resistors on the input circuits as shown in Figure 2-2 on page 16.

Warnings and Cautions

WARNING **SHOCK HAZARD. Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the switch module. Before you remove any installed module, disconnect AC power from the mainframe and from other modules that may be connected to the modules.**

Caution **STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components in the switch module, observe anti-static techniques whenever removing a module from the mainframe or whenever working on a module.**

Installing in a VXI Mainframe

The Agilent E6174A Event Detector Module can be installed in any available mainframe slot except slot 0.

Setting the Address Switch

The logical address switch (LADDR) factory setting is 8. You may have to change the setting during module installation. Valid address values are from 1 to 254. Figure 1-1 shows the switch location and factory setting.

Setting the Interrupt Level

Many VXI modules generate an interrupt to indicate that a command has completed. These interrupts are sent to, and acknowledged by, the Agilent Command Module or other system controller via one of seven VXI backplane interrupt lines. Different controllers treat interrupt lines differently, and you should refer to your controller's documentation to determine how to set the interrupt level jumpers on your module.

Note Many mainframes have backplane switches or jumpers for the interrupt lines. If your mainframe is of this type, make certain those switches or jumpers are open for the slot where the module is installed.

Agilent Command modules configured as VXI Resource Managers (i.e. logical address set to 0) treat all interrupt lines as having the same priority. For interrupters using the same line, priority is determined by which mainframe slot the module is installed in. Lower-numbered slots have higher priority than higher-numbered slots. Agilent Command Modules

service line 1 by default, so it is normally correct to leave the module's jumpers at the factory setting of 1. If in doubt, refer to your Command Module's User's Manual.

If your controller's documentation instructs you to change the interrupt level, refer to Figure 1-1. To cause the module to interrupt on one of the VXI interrupt lines (1 through 7), put the jumper in the position with the same number. To disable the module's interrupt, put the jumper in the "X" position. If your module has two 2-pin jumpers instead of one 4-pin jumper, make certain both jumpers are in the same position.

Note Moving the interrupt level jumper from its factory default position of 1 is not recommended. Do not place the jumper in the X position if you are using an Agilent Command Module.

Chapter 2
Understanding the Agilent E6174A 32-Channel Event Detector Module

Using This Chapter

This chapter contains information about the operation of the Agilent E6174A 32-Channel Event Detector Module. It contains the following sections:

Block Diagram

Figure 2-1 is a logic block diagram of the Agilent E6174A 32-Channel Event Detector. Figure 2-2 shows a detail of the input signal conditioning section.

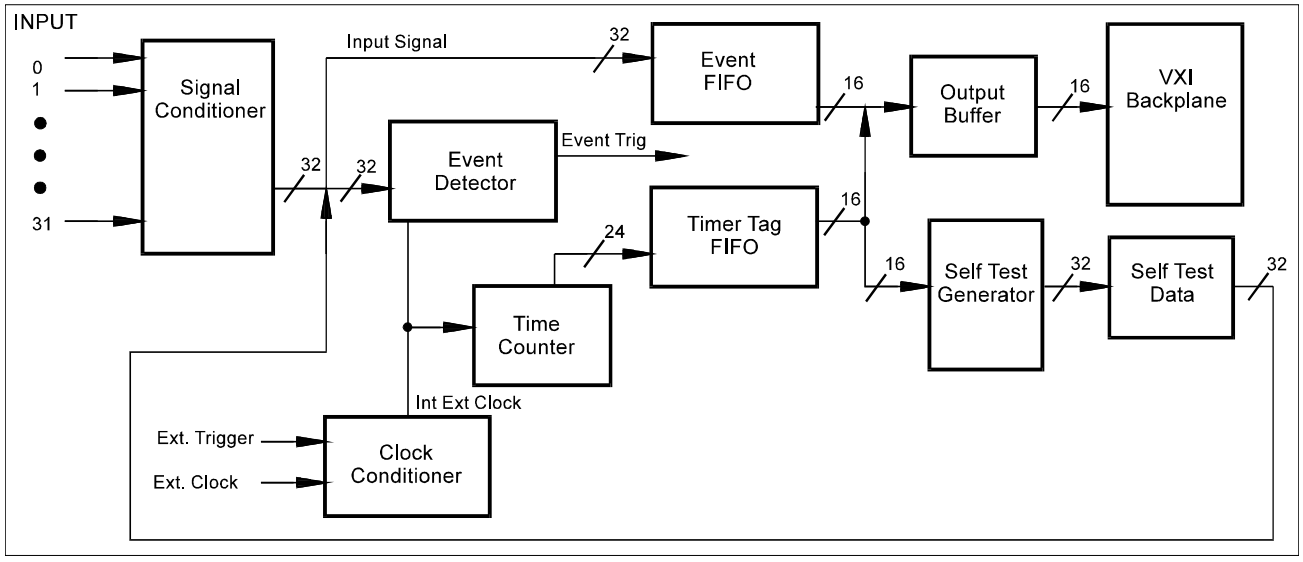

Figure 2-1. Functional Block Diagram of 32-Channel Event Detector

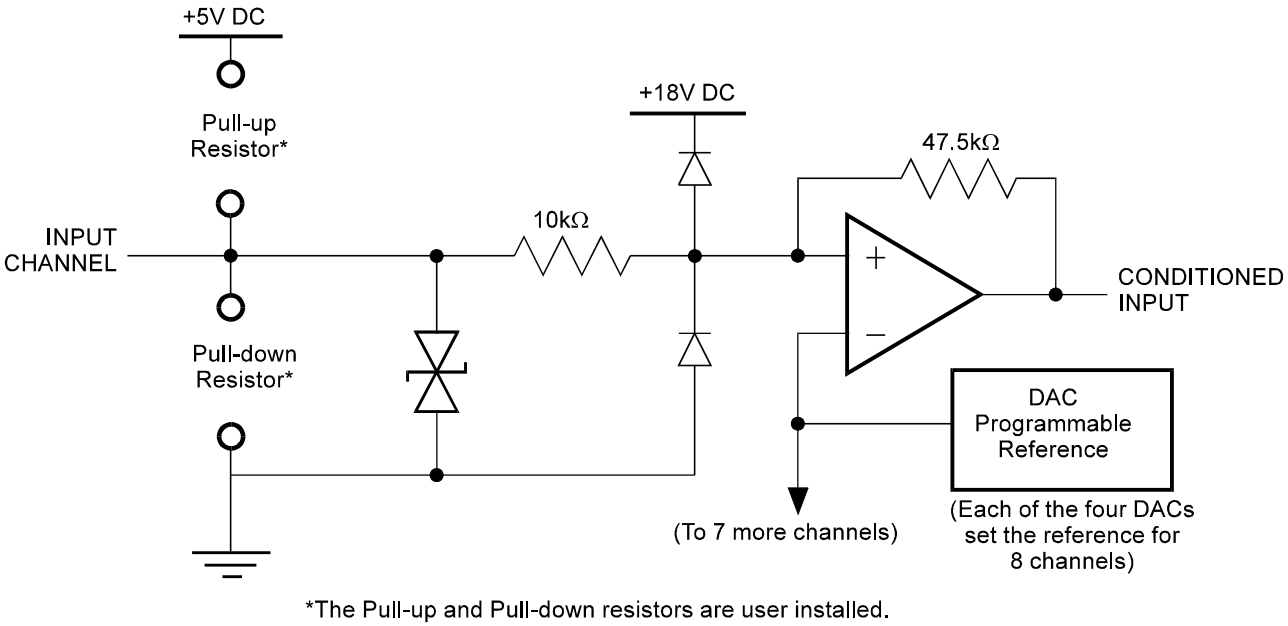

Figure 2-2. Detail of Input Conditioning, including User Installable Pull-Up/Down Resistors

Description of Features

The Agilent E6174A is a 32-Channel input event detector that records and time stamps all the input channels' status any time any input level changes.

The Module is equipped with input conditioning, user installable pull-up or pull-down jumpers on each channel, and four programmable 8 bit DAC Reference Generators. The system has a base clock rate of 10 MHz with a four decade divider, providing a programmable clock and trigger selector, as well as provisions for an external trigger and clock.

The system is equipped with a self-test generator that verifies the functionality of the module between the input to the event detector and the output of the Event and Time Tag FIFO's.

Input Signal Conditioning

Refer to Figure 2-2. Each input channel is fed to the + side of an input comparator. Each input can have a user installed pull-up resistor to +5 V or a pull-down resistor to ground. The output of each channel's comparator is fed to the 32-channel event detector circuitry.

If the user wishes to install the appropriate resistor to pull-up or pull-down a channel, Table 2-1 gives the resistor number for the appropriate channel for both pull-up and -down functions.

Table 2-1. Input Conditioning Resistor Assignments

Channel No.	Pull-Up Resistor Number	Pull-Down Resistor Number		Channel No.	Pull-Up Resistor Number	Pull-Down Resistor Number
0	R1001	R1002		16	R2001	R2002
1	R1011	R1012		17	R2011	R2012
2	R1021	R1022		18	R2021	R2022
3	R1031	R1032		19	R2031	R2032
4	R1041	R1042		20	R2041	R2042
5	R1051	R1052		21	R2051	R2052
6	R1061	R1062		22	R2061	R2062
7	R1071	R1072		23	R2071	R2072
8	R1081	R1082		24	R2081	R2082
9	R1091	R1092		25	R2091	R2092
10	R1101	R1102		26	R2101	R2102
11	R1111	R1112		27	R2111	R2112
12	R1121	R1122		28	R2121	R2122
13	R1131	R1132		29	R2131	R2132
14	R1141	R1142		30	R2141	R2142
15	R1151	R1152		31	R2151	R2152

* Note: The user-installed Pull-up/Pull-down resistors should be 1/8 watt, 1Kohm.

DAC Input Reference Generators

The DAC threshold values can be from 0 to 15 volts with 8 bits resolution. The four DACs serve as reference generators setting the threshold of each comparator. The following table shows which channels' threshold are controlled by which of the four DACs.

Note that the DAC resolution is about 60 mv, and the input condition circuitry hysteresis is about 450 mv. The degree of resolution is greater than the accuracy permitted by the hysteresis.

Table 2-2. J3 Pin Assignments

Channel No.	J3 Conn. Pin No.	J3 Conn. Pin No.	Reference Voltage Group
31	1	2	DAC #0 (Register 28)
30	3	4	
29	5	6	
28	7	8	
27	9	10	
26	11	12	
25	13	14	
24	15	16	
23	17	18	DAC #1 (Register 2A)
22	19	20	
21	21	22	
20	23	24	
19	25	26	
18	27	28	
17	29	30	
16	31	32	
15	33	34	DAC #2 (Register 24)
14	35	36	
13	37	38	
12	39	40	
11	41	42	
10	43	44	
9	45	46	
8	47	48	
7	49	50	DAC #3 (Register 26)
6	51	52	
5	53	54	
4	55	56	
3	57	58	
2	59	60	
1	61	62	
0	63	64	

* Note: All even numbered pins are grounded

32-Channel Event Change Detector

The 32 channel Event Detector consists of two D flip-flops in series on each channel. The D flip-flops are clocked by the same clock signal that also clocks the 24 bit timer. The output of the first flip-flop is XOR'd with the output of the second flip-flop. If a change occurs in the signal on that channel, the output of the first and second flip-flop will for one clock cycle at least, be different. This difference in the two signals will cause the XOR to go high. All of the outputs from the 32 XORs are cascaded into a single OR gate. The output of the XOR's is normally 0, so the output of the trigger is normally low. Any signal going high drives the event trigger (essentially a 32 input OR gate) high as well.

When any channel experiences a change in value, the event trigger causes the current data on the first set of flip-flops to be written to the Event FIFO, and the value of the 24 bit timer to be written to the Time Tag FIFO.

The event detector has an internal programmable clock and trigger, as well as jacks for an external clock and trigger.

System Clock and Timer Resolution

The Event Detector is equipped with both a four decade selectable internal clock and an external clock input. The maximum system clock rate for the system, whether external or internal source, is 10 MHz.

The 24 bit system timer allows a test duration of 16,777,215 clock cycles (2^{24}-1) before the system generates a “Register Full” flag and halts event processing.

Table 2-3. System Clock and Timer Resolution

Clock Rate	Resolution	Time Range
10 MHz	0.1 µsec/tic	1.6 sec.
1 MHz	1 µsec/tic	16.7 sec.
100 kHz	10 µsec/tic	167 sec. (2 min. 47 sec)
10 kHz	100 µsec/tic	1677 sec. (27 min. 57 sec)

Note that “glitches” and transients that last less than a clock cycle may not be detected unless they span the clock hi-low transition portion of the clock signal. If a transient occurs and terminates within the same half clock cycle, it may not be detected.

Self-Test Generator

The self-test software is not generally available on all systems yet. However, the software functions as follows. It generates a pattern of “walking ones” that are fed into the card input just after the input conditioner circuitry. Since each succeeding pattern set is different than the previous one, the event change is detected, and the walking ones pattern and the associated time stamp to be recorded in the Data and Time Stamp FIFOs. The test is complete once the FIFOs are filled (1024 events) and the results analyzed. If an erroneous datum or time stamp is detected, the failure is recorded by the system. Self-test requires approximately 16 seconds to complete.

Reset When the FIFOs are full, or the clock has completed it's 24 bit count, the system is halted, and data processing is stopped until a reset command is issued by the VXI bus, or the card undergoes a power-on reset.

Chapter 3
Using the Agilent E6174A 32-Channel Event Detector

Using This Chapter

This chapter contains the following sections:

- Reset State
- Programming

Reset State

The Agilent E6174A module resets to its default state whenever:

- Operating power is first applied.
- Operating power is removed and then reapplied.
- Bit 0 in the Control register (described in Appendix B) is asserted.

Programming

Your programmatic interaction with this module is done via the VXIbus system controller. Refer to its documentation for more information.

Sample Program

The following pseudo-instructions give a sense of how the event detector is used in a system.

```
SETUP FOR EVENT TEST
INITIALIZE EVENT DETECTOR
Define the logical address for event detector
Check card manufacturer (Register 0) and model ID (Register 2).
Reset C/S register 04h (toggle bit 0 lo, hi, lo)
 Write to Register 04, RESET=0
 Write to Register 04, RESET=1
 Write to Register 04, RESET=0
Verify C/S Register 04h contents is reset to (1110001100111111) or E33Fh
SETUP EVENT DETECTOR
Select clock and trigger mode in Trigger/Clock
Select Register 20h (set values for External clock, or internal clock and the
internal clock rate, also select to trigger on rising or falling clock signal,
and optional gate control)
Set input voltage reference (VREF) levels
 Write to DAC registers, set desired input threshold voltage.
   Register 24h - VREF 2, Channels 8-15
   Register 26h - VREF 3, Channels 0-7
   Register 28h - VREF 0, Channels 24-31
   Register 2Ah - VREF 1, Channels 16-23
PERFORM MEASUREMENTS WITH EVENT DETECTOR.
Set the test enable bit ISTART=1, on Register 22h, to enable sampling to begin.
When the FIFO's Empty Bit, register 04h bit 13, is NOT set (0), download the
FIFOs to the VXIbus via the data registers
 (Registers 30h & 32h) and the time stamp registers (Registers 34h & 36h)
Use either a looping counter or interrupt-based software scheme to count the
elapsed time, and check interrupts and warning flags.
 IF a FIFO full flag occurs (bit 12 = 1 on Register 04h)
   Disable the inputs and keep disabled until the card is reset.
   Write FIFO contents to the VXI controller.
   Write a FIFO Overflow warning to the standard output.
```

Appendix A
Agilent E6174A Event Detector Specifications

General

Module Size/Device Type: C-Size VXIbus, register based, A16/D16

Operating Temperature: 0 to 55 °C

Operating Humidity: 65% RH, 0 to 40 °C

Memory Depth: 1024 Events

Data Lines

Minimum Input Pulse Width: 200 nS

Input Voltage Range: 0 to +15V

Channel Input Impedance: 55kΩ

Channel Input Hysteresis: ≅0.87V

External Clock

Maximum Speed: 10MHz

Maximum Pulse Width: must be greater than 0.1 µS

Input Levels: TTL

External Gate

Threshold Level: TTL

Input Pull-up Resistor: 1kΩ

Notes:

Appendix B
Register Definitions

Addressing the Registers

To access a specific register for either read or write operations, you must use its register address. Register addresses for VXIbus plug-in modules reside in an address space called "A16" whose size is $FFFF_h$. The exact location of the A16 address space within a VXIbus master's memory map depends on the system resource manager.

VXIbus modules are addressed at locations above C000h within the A16 address space. Because each module requires one 64 byte (40_h) block of addresses, the A16 address space between C000h and $FFFF_h$ can accommodate as many as 254 VXIbus modules.

Given the address space of each module is 64 bytes, the module address is determined by its logical address (set by the address switches) multiplied by an offset of 64 (40_h). Suppose the A16 address space began at $1F0000_h$ and the Agilent E6174A module's address is 10 (A_h). Then the addresses of the module's internal registers—i.e., the base address of the module—would start at $1FC280_h$, like this:

$$1F0000_h + C000_h + (A_h * 40_h) = 1FC280_h$$

A16 Address Space Outside the System Controller When the A16 address space is outside the system controller, the base address of the Agilent E6172A module is computed as:

$$A16_{base} + C000_h + (LADDR_h * 40_h)$$

or (decimal)

$$A16_{base} + 49{,}152 + (LADDR * 64)$$

where $C000_h$ (49,152) is the starting location of the register addresses, LADDR is the module's logical address, and 64 is the number of address bytes per VXIbus device. For example, if the Agilent E6174A's logical address (LADDR) was set to 10 (A_h), it would have a base address of:

$$A16_{base} + C000_h + (A_h * 40_h) = C000_h + 280_h = C280_h$$

or (decimal)

$$A16base + 49{,}152 + (10 * 64) = 49{,}152 + 640 = 49{,}792$$

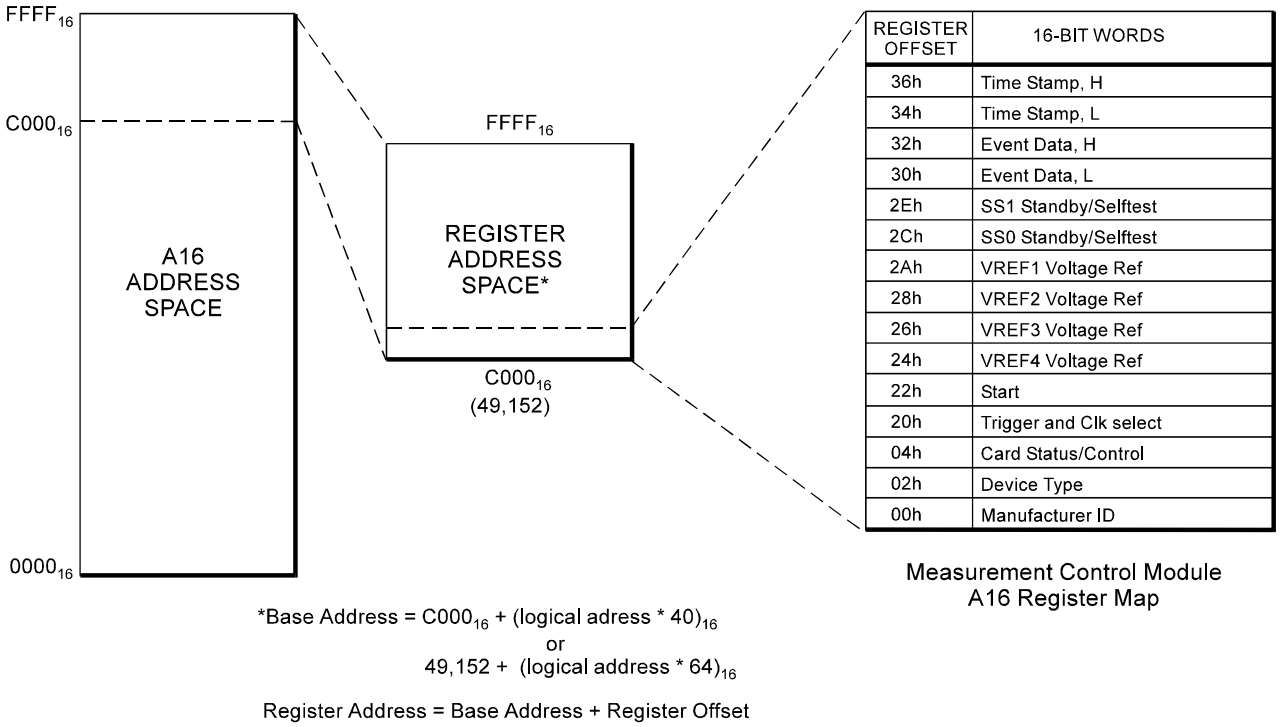

Figure B-1. Register Locations Within the A16 Address Space

Register Offset

The offset for a specific register is that register's location in the block of 64 address bytes that belongs to the module. For example, the module's Status/Control Register has an offset of 04_h. Continuing with the previous example, whose base address was $1FC280_h$, when accessing this register, you would add the offset to the base address to form the register address, like this:

$$1FC280_h + 04_h = 1FC284_h$$

or (decimal)

$$2{,}088{,}448 + 10 = 2{,}088{,}458$$

Register Descriptions

The Agilent E6174A 32-Channel Event Detector has the following registers:

- Manufacturer ID Register (base + 00_h)
- Device Type Register (base + 02_h)
- Status/Control Register (base + 04_h)
- Internal Trigger and Clocks register which is:
  -- RR0 Internal Triggers and Clock selection (base + 20_h)
- Start Register:
  -- RR1 RISTART (base + 22_h)
- Programmable input voltage reference registers:
  -- RR2 VREF2 (base + 24_h)
  -- RR3 VREF3 (base + 26_h)
  -- RR4 VREF0 (base + 28_h)
  -- RR5 VREF1 (base + $2A_h$)
- Standby and Selftest Registers:
  -- SS0 Standby (base + $2C_h$)
  -- SS1 Selftest (base + $2E_h$)
- Event Data Registers:
  -- DR0 REVNTDATAH (base + 30_h)
  -- DR1 REVNTDATAL (base + 32_h)
- Time Tag Registers:
  -- DR2 RTTAGU (base + 34_h)
  -- DR3 RTTAGL (base + 36_h)

Manufacturer Identification Register

The Manufacturer ID Register is a 16-bit read-only register at address 00_h with the most significant byte (MSB) at 00_h and the least significant byte at 01_h. Reading this register returns $FFFF_h$, which identifies this module as register-based, A16-only, and made by Agilent Technologies .

Device Type Register

The Device Type Register is a 16-bit read-only register at address 02_h with the most significant byte (MSB) at address 02_h and the least significant byte (LSB) at address 03_h. Reading this register returns 0156_h, which uniquely identifies this module as an Agilent E6174A.

Status/Control Register

The Status/Control Register is actually two independent registers at a single address. The readable or "status" portion of the register returns information about the current state of the module. The writable or "control" portion of the register controls various functions of the module. The bit fields of the register are described below, along with the definitions of terms unique to them. Only bits 0, RESET, and 6, Disable Interrupts, are writable. All the other bits are read-only.

Status Register (base + 04_h)

Bit	15	14	13	12	11	10	9	8
Purpose	Undefined	MODID	EPFLG	FLFLG	HFFLG	OFFLG	Undefined	Undefined
Value	1	0	1	0	0	0	1	1

Bit	7	6	5	4	3	2	1	0
Purpose	User Inter-rupts	Disable Inter-rupts	Unde-fined	Unde-fined	Unde-fined	Unde-fined	Unde-fined	RESE T
Value	0	0	1	1	1	1	1	0

* After an initial transition at power-on, the default state of this register is $A33E_h$.

* The Empty, Half-full, and Full flags of all seven FIFOs are respectively OR'd together, so that a change in any one of them will set that respective flag.

MODID: "0" indicates the module is present. Used only during configuration.

EPFLG: FIFO register is empty. A "1" indicates the register has no data.

FLFLG: FIFO register is full. A "1" indicates the registers are full and the Agilent E6174A will stop recording data.

HFFLG: FIFO register is half-full. A "1" indicates the register is half full of data.

OFFLG: This flag is generated when the FLFLG is set. A "1" indicates that the IRQ line has been disabled, suspending further data recording.

undefined: All undefined bits appear as "1" when read.

User Interrupt: "1" indicates either a Counter or Event error occurred.

Disable Interrupts: "1" disables interrupts.

RESET: Normally "0", setting the state to "1" resets the system counters, FIFOs, etc.

The proper sequence for resetting the card is to write "0", then "1", and then "0" again. Note that the reset bit must be cleared after asserting it or the module will be in a perpetual state of reset.

Trigger & Clock Select Register

The Trigger and Clock Select Register enables you to select between external and internal clocks, the internal clock speed (4 decades from 10 MHz to 10 Khz), the trigger edge to initiate data collection on, rising or falling, and the control bit to start/stop data collection.

Trigger and Clock Select Register (base + 20_h)

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	ICLK1	ICLK0

Bit	7	6	5	4	3	2	1	0
Signal	X	X	X	X	X	CLKSEL	TRGEDGE	STSTSEL

ICLK1 and ICLK0: These two bits select the internal clock rate according to the following scheme:

Bit 9	Bit 8	Clock Rate
0	0	10 MHz
0	1	1 MHz
1	0	100 Khz
1	1	10 Khz

CLKSEL: This bit selects between the Internal Clock, "0", and the External Clock, "1".

TRGEDGE: Selects which edge of the External trigger to initiate from. "0" selects rising edge to Start and "1" to Stop; "1" selects falling edge to Start and "0" to stop.

STSTSEL: Start/Stop select bit. This is the Gate enable control: "0" is Internal, and "1" is External.

Start Register

The start register only uses two bits, bit 8 which indicates if either a count error or event error has been set, and bit zero, which is set to initiate a test using the internal start/stop gate.

Start Register (base + 22_h)

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	USERINT

Bit	7	6	5	4	3	2	1	0
Signal	X	X	X	X	X	X	X	ISTART

USERINT: Reflects CUNTERR and EVNTERR.

ISTART: Internal gate start/stop bit: 0=Stop, 1=Start. This bit must be enabled in order to run any test

Voltage Reference Registers

The Agilent E6174A has four 8-bit programmable input voltage reference D/A Converters (DAC), one for each bank of eight inputs. The output range is:

Ref.	Voltage Level
00_h	0 Volts
FF_h	15 Volts =0/-5% Tolerance
Resolution is 58.8 mV/bit.	

For Example: In order to output 1V offset, the register would be set to 17 decimal or $FF11_h$ (1 Volt / .0588 V/count = 17 count)

During module reset, the 0V data is written to all four DACs.

VREF2 Voltage Reference Register (base + 24_h): Channels 8-15

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signal	REFB 7	REFB 6	REFB 5	REFB 4	REFB 3	REFB 2	REFB1	REFB0

VREF3 Voltage Reference Register (base + 26_h): Channels 0-7

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signa	REFB 7	REFB 6	REFB 5	REFB 4	REFB 3	REFB 2	REFB1	REFB0

VREF0 Voltage Reference Register (base + 28_h): Channels 24-31

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signal	REFB 7	REFB 6	REFB 5	REFB 4	REFB 3	REFB 2	REFB1	REFB0

VREF1 Voltage Reference Register (base + $2A_h$): Channels 16-23

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signal	REFB 7	REFB 6	REFB 5	REFB 4	REFB 3	REFB 2	REFB1	REFB0

Standby & Selftest Registers

The self test register is used when the card performs self-test. Only bits 5, 6, and 7 are actually used by the card.

SS0 Standby Register (base + $2C_h$)

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signal	X	X	X	X	X	X	X	X

SS1 Selftest Register (base + $2E_h$)

Bit	15	14	13	12	11	10	9	8
Signal	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Signal	ONTEST	COUNTERR	EVENTERR	X	X	X	X	X

ONTEST: 0 - Selftest not currently being run.
1 - Selftest in progress.

COUNTERR: 0 - No error detected in the timer.
1 - Error detected in timer count.

EVENTERR: 0 - No error detected in selftest data comparator.
1- Error detected in selftest data comparison.

Event Data Registers

These two registers transfer the Input Status data from the data FIFO to the VXI data bus. This data is downloaded from the FIFO in First-in, First Out order.

Event Data Register (High) (base + 30_h)

Bit	15	14	13	12	11	10	9	8
Signal	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24

Bit	7	6	5	4	3	2	1	0
Signal	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

Event Data Register (Low) (base + 32_h)

Bit	15	14	13	12	11	10	9	8
Signal	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

Bit	7	6	5	4	3	2	1	0
Signal	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CHnn: State data on the specified Input Channel number at associated time t in the Time Tag Registers.

Time Tag Registers

These registers transfer the Time Tag data that is loaded from the Time Tag FIFO.

Time Tag (High) Register (base + 34_h)

Bit	15	14	13	12	11	10	9	8
Signal	EF	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Signal	TCB23	TCB22	TCB21	TCB20	TCB19	TCB18	TCB17	TCB16

Time Tag Register (Low) (base + 36_h)

Bit	15	14	13	12	11	10	9	8
Signal	TCB15	TCB14	TCB13	TCB12	TCB11	TCB10	TCB9	TCB8

Bit	7	6	5	4	3	2	1	0
Signal	TCB7	TCB6	TCB5	TCB4	TCB3	TCB2	TCB1	TCB0

EF: Empty Flag, "0"= FIFOs are NOT empty, "1"= FIFOs are empty.

TCBnn: These are the 24 Time tag data bits associated with the Event Data in the Event Data Registers.

Notes: